80dB CMRR and 70dB PSRR Analog Front-end Integrated Chip and Digital Signal Processing Algorithm for a ECG Acquisition System

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ABSTRACT—This paper presents an acquisition system design integrated with DE0 Nano platform and the proposed analog front-end (AFE) for the prototype development of a portable ECG signal monitor. The result shows that a pure ECG signal can be easily acquired by the proposed design. Therefore, it would be very suitable for the integrated chip design of ECG signal processor in the future.

I. PROPOSED ARCHIECTURE DESIGN OF ECG SIGNAL ACQUISITION SYSTEM

In this work, we present an acquisition system design integrated with a front-end integrated chip and FPGA, as shown in **Fig. 1**, for the development of a portable ECG signal recorder. An 80dB common mode rejection ratio (CMRR) and 90dB power supply rejection ratio (PSRR) guaranteed differential difference instrument amplifier (IA), as shown in **Fig. 2**, and rail-to-rail OPA designs, as shown in **Fig. 3**, are all employed to the proposed analog front-end (AFE) integrated chip.

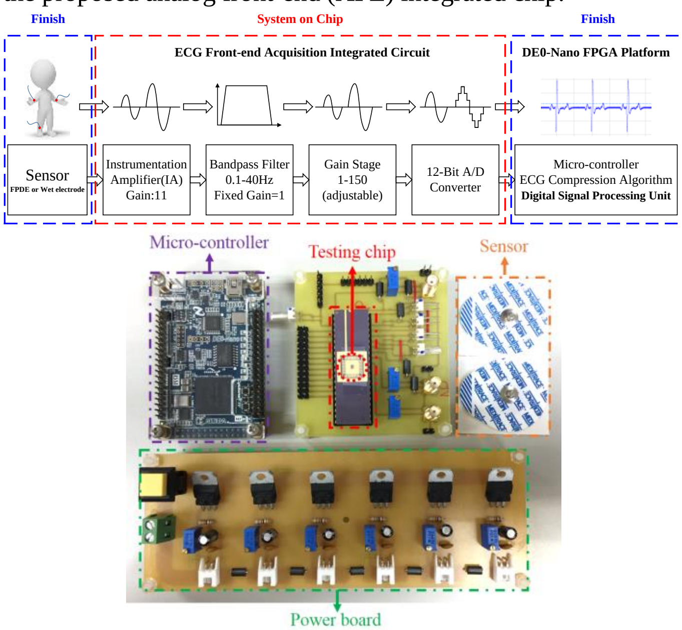
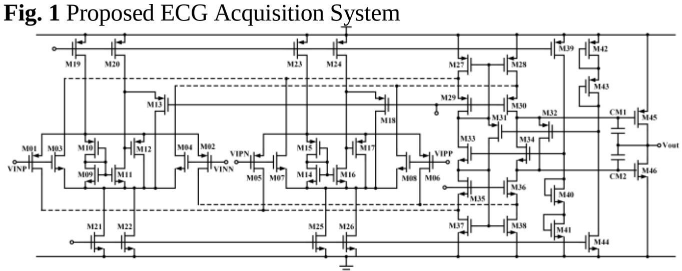


Fig. 1 Proposed ECG Acquisition System



(a)

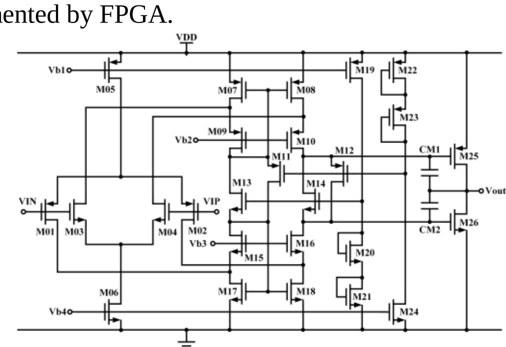
SPECIFICATION AND MEASUREMENT

Item.	Post-sim	Measurement
Power Supply	1.8	1.8
Output Swing	0~1.8	0.2~1.69
CMRR	110	80dB
PSRR	101	90dB

(b)

Fig. 2 Proposed Differential Difference Instrument Amplifier

The proposed AFE design also involves a band-pass filter, a gain stage circuit, and a 10-bit guaranteed successive approximation ADC. **Figs. 4** and **5,** respectively, show the band-pass filter design and SAR ADC. The output of the IA follows the band-pass filter, which adopts 2-order Sallen-Key topology. The cut-off frequency is set at 40Hz to reduce high-frequency noise. The output of AFE is connected to Altera DE0 nano FPGA platform for ECG signal processing. ARM processor can execute a program for 60Hz power line interference (PLI) cancellation with a hardware accelerator implemented by FPGA.



(a)

SPECIFICATION AND MEASUREMENT

Item.	Post-sim	Measurement
Power Supply	1.8	1.8
Output Swing	0~1.8	0.18~1.71
CMRR	137	90dB
PSRR	91	70dB
Gain	1~100	1~100

(b)

Fig. 3 Proposed Rail-to-Rail OPA Design

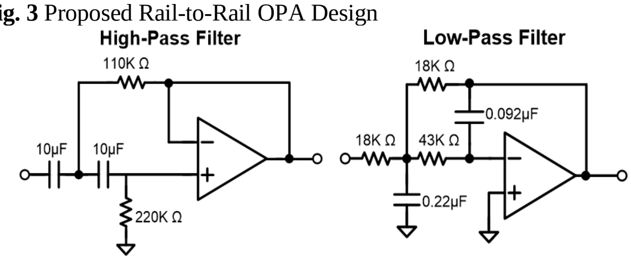


Fig. 4 Proposed Band-pass Filter Design

II. Sliding Discrete Fourier Transform Based NLMS Algorithm for PLI Cancellation

Figure **6(a)** demonstrates the proposed sliding discrete Fourier transform based normalized least mean square filter (SDFT-NLMS) improved form FFT-LMS [1, 2], which can be combined with our previous works [3, 4] by a low-complexity SDFT algorithm. The system transfer function of SDFT is shown as

$$H_{Lai}(z) = \frac{j\sin(\theta_k) + (\cos(\theta_k) - z^{-1})}{1 - z^{-1}(2\cos(\theta_k) - z^{-1})}. \quad (1)$$

Figure **6(b)** shows the compact SDFT computation. The acquired ECG signal is fed into the $d(n)$ point, a pure 60Hz sine wave is fed into the $x(n)$ point, and the $e(n)$ point is the output signal while the SDFT-NLMS achieve convergence.

III. Realization Results

Table I compares mean square error (MSE) value for various well-known adaptive filtering algorithms under the same conditions, where the interference of 60Hz sine wave has 100mV amplitude, the desired signal is with a -30dB white noise generated by Matlab's function of awgn(sinewave, 30), and the pure 60Hz sine wave has 10mV amplitude, the order of LMS is 128, and the values of "*mu*" and "*a*" are, respectively, "0.01" and "0.00000001".The results show that the proposed SDFT-NLMS eventually has better performance, and **Fig. 7** demonstrates the frequency spectrum results of various LMS adaptive filtering algorithms for MIT-BIH ECG signal recorded (data#119 samples are ranged from 1 to 10080) with 60Hz PLI. It also proved that 60Hz PLI can be greatly reduced from 27.33 dB into 8.06 dB.

Table I.
Comparison of Mean Square Error for Various Algorithms

Algorithm	Mean Square Error with Different Noise Levels		
	100 mV	200 mV	300 mV
LMS	0.01305	0.02375	0.04166
NLMS	0.00957	0.00974	0.00998
SDFT-LMS	0.00959	0.00987	0.01030
SDFT-NLMS	0.00954	0.00967	0.00983

References

[1] L. Jae and U. Chong, "A reduced structure of the frequency-domain block LMS adaptive digital filter," *Proceedings of the IEEE*, vol. 72, pp. 1816-1818, 1984.

[2] J. J. Shynk, "Frequency-domain and multirate adaptive filtering," *IEEE Signal Processing Magazine*, vol. 9, pp. 14-37, 1992.

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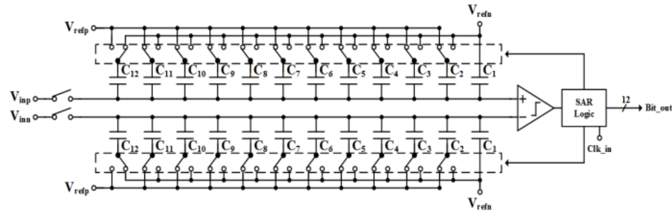
[4] W.-H. Juang, S.-C. Lai, K.-H. Chen, W.-k. Tsai, and C.-H. Luo, "Low-complexity hopping DFT design based on a compact recursive structure," *Electronics Letters*, vol. 53, no. 1, pp. 25–27, Jan. 2017.



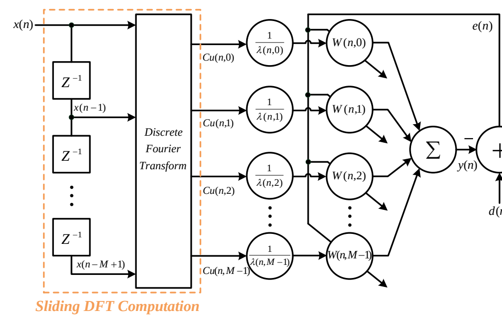
(a)

Specification and Measurement

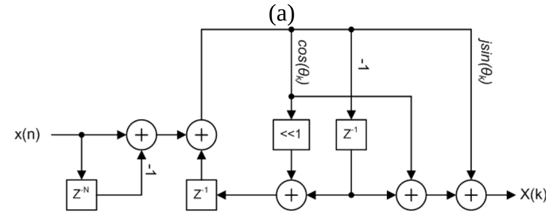
Item	Post-sim	Measurement
Power Supply	1.8	1.8
Sampling Frequency	200KHz	31.25KHz
Fin(nper*Fs/N)	5.17KHz	1.291KHz
N	2048	16384
nper	53	677
SNDR	70.92dB	62.19dB
ENOB	11.49Bit	10.03Bit

(b)

Fig. 5 Proposed 12-bit SAR Design



(a)



(b)

Fig. 6 Proposed Low-Complexity SDFT-NLMS Algorithm: (a) SDFT-NLMS Algorithm; (b) Low-Complexity SDFT computation.

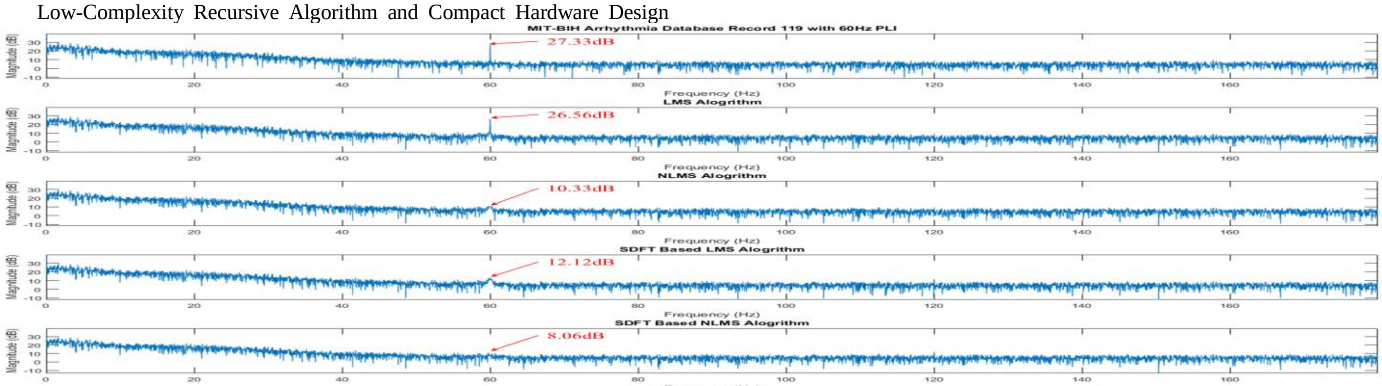


Fig. 7 Frequency spectrum results of various LMS adaptive filtering algorithms for MIT-BIH ECG signal with 60Hz PLI.