A Digitally Self-Calibration Method with Recursive DFT Algorithm for 12-bit SAR ADC Realization

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***Abstract* —This paper presents a digitally self-calibration method with a recursive discrete Fourier transform (RDFT) algorithm for successive approximation (SAR) analog-to-digital converters (ADCs). A behavior model of 12-bit SAR ADC based on Matlab Simulink is proposed to combine with the compensation algorithm and digital input testing signal. In addition, the SAR ADC error caused by 1% capacitor mismatch of the DAC array is also built for evaluation of the real radixes of the DAC capacitor array. The proposed digital calibration method utilizes a RDFT to detect the third harmonic distortion value and to evaluate the error factor by using the calibration formula. Then, the error factor is applied to generate a new digital output code for the targeted SAR ADC. Under the sampling rate of 126.26 S/s, the simulation results reveals the third harmonic distortion is -47.98 dB before calibration and -84.34 dB after calibration with 1% capacitor mismatch. In addition, the SNDR and ENOB can be enhanced to 20.9 dB and 3.52 bit, respectively. Therefore, the proposed method can be adopted to enhance the performance of the ADC for various applications in the future.**

Keywords: Digital calibration method, Recursive DFT, Self-calibration

I. INTRODUCTION

Analog-to-digital converter (ADC) is an important component in various areas, such as communication system, biomedical system and so forth. The performance limitations of ADCs are mainly dominated by the static and dynamic nonlinear effects which cause the harmonic distortion in the output power spectrum. These nonlinearities slightly deteriorate the overall system performance. In addition, because of the technology scaling into the nanoscale region, it increases the sensitivity to the process variation and system interference noise. Therefore, the calibration method becomes very necessary for ensuring the system quality. The SAR ADC has the advantages of the medium speed conversion and medium to high resolution, so it is more suitable for the biomedical and communication systems [1,2]. However, the capacitor mismatch of the DAC array and the DC offset of the comparator, which caused by the process variation, are two critical performance limitations for the SAR ADC. In order to overcome the capacitor mismatch and DC offset, many calibration methods have been published in recent years. As mentioned before [3], the nano-scale device has the advantage of high speed, full integration and low power. Thus, the digital calibration method becomes more popular. As a consequence, we only focus on the digital calibration method in this topic. For instance, the lookup-table technique is the most common method for static error correction [4]. In Chang *et al.*'s work, a corrected ADC output was produced by using the lookup table, where pre-calculated values are stored in the memory. However, the main disadvantage is an amount of memory requirement for the calibration, *i.e.* the limited capability of correcting the error for previously measured and stored.

Another approach called dithering skill [5] is a well-known digital calibration method. The weights of the most significant bit (MSB) capacitor can be measured by adding a stimulus to the desired signal at ADC input, and then were removed by low-pass filtering output signal. However, some nonlinearity effects are not addressed, such as charge injection and on-resistance error of the track-and-hold device. The dithering method cannot be applied to deal with these problems. As a result, model inversion is published to overcome the drawback of dithering method, but it requires more complex architecture for practical applications.

In Schmidt *et al.*'s work [6], the post-compensation method is used for compensator model, such as the memory polynomial (MP) and modified MP, to compensate the nonlinearity error. Based on this work, the original ADC output data was measured by using the compensator, and then was corrected with an extra ideal ADC circuit [6]. The drawbacks of this skill is depended on a more complex and high-precision model, which is very difficult for practical implementation. Recently, an internal redundancy dithering (IRD) technique is reported in [7]. The IRD method based on the bit-weight calibration employs a pseudorandom bit sequence to determine the threshold values and utilizes the least mean square (LMS) algorithm to calibrate the error of SAR ADC. Compared with other LMS-based approaches, the advantages of Wang *et al.* [7] not only can reduce the convergence time of calibration algorithm but also can improve the linearity of ADC. However, the main drawback is that an ideal ADC is required in implementation. On the other hand, it is worthy to mention that a fast Fourier transfer (FFT)-based calibration method was proposed for the pipeline ADC to calibrate the capacitor mismatch and the finite gain of the OPAMP [8]. However, the shortcoming of the FFT process consumed more power because all frequency bins should be computed during the operation mode. To overcome this problem, Juan *et al*. proposed a RDFT-based calibration algorithm [9].

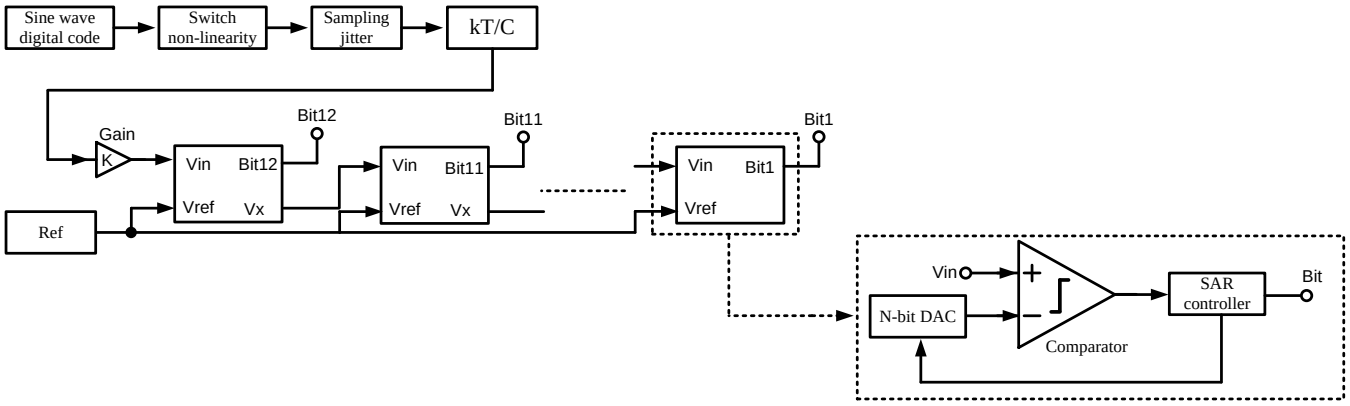


Fig. 1. Block diagram of 12-bit SAR ADC.

Based on the previous works [8, 9], we further presented a digitally self-calibration technique to compensate the error by using the simplified digital calibration algorithm. In addition, the advantage of the RDFT owns variable transform length, lower computational complexity and less hardware cost in realization. To verify the proposed method, a 12-bit SAR ADC and RDFT process are both co-simulated by using the Matlab Simulink. The simulation result reveals that the third harmonic distortion could be clearly reduced from -47.98 dB to -84.34.

The rest of this paper is organized as follows: Section II briefly reviews the proposed calibration formula and describes the digitally self-calibration flow. The concept of the proposed method is also presented in Section II. The simulation result is shown in Section III. Finally, conclusions are outlined in Section IV.

II. Proposed Self-Calibration Algorithm

A. The proposed calibration formula

Previous work [9] derived the calibration formula by using the Fourier series and a cosine wave for the input signal. An evaluation of the 3rd harmonic distortion value, *i.e.* a_3, can be further used to calculate the error factor Δ_n. This previous work also proved that the effects of capacitor mismatch and DC offset for ADC could be greatly reduced. In addition, the calibration code was only used for the first-time test. The main calibration equation could be addressed as:

$$a_3 = 20\log\left(\frac{A\times\Delta_n\times 1.696\times C_n}{2048} + 1.696\times V_{os}\right) \quad (1)$$

, where A is the amplitude of the cosine wave, Δ_n is the error factor of each capacitor mismatch, and the V_{os} is the DC offset. Here, we assume that A=1 and the DC offset (V_{os}) is 0.5mV, and the relationship between a_3 and Δ_n is rewritten as:

$$\Delta_n = \frac{\left(10^{p} - 0.000848\right)\times 2048}{1\times 1.696\times C_n},\ p = a_3/20. \quad (2)$$

In this work, we substitute the value of a_3 as the real part and imaginary part, Eq. (2) can be further simplified as:

$$\Delta_n = \frac{(10^{\frac{1}{2}\log\sqrt{(\mathrm{Im})^2+(\mathrm{Re})^2}} - 0.000848)\times 2048}{1\times 1.696\times C_n}, n = 11\sim 0 \quad (3)$$

In this sense, we can calculate the error factor (Δ_n) by Eq. (3), and the final correction code which can be utilized to compensate the error is further obtained as:

$$D_{new} = Bit12\times 2^{11}\times\left(2\pm\Delta_{12}\right) + Bit11\times 2^{10}\times\left(2\pm\Delta_{11}\right) + \cdots Bit2\times 2^{1} + + Bit1\times 2^{0}. \quad (4)$$

While the compensation is finished, the residue errors are not always compensated. The minimum residue error should be therefore corrected by fine tune. Finally, we can use this calibration method to suppress the third harmonic distortion of ADC and to enhance the ADC's performance, respectively.

Figure 1 shows the simple block diagram of a 12-bit SAR ADC Matlab Simulink model. The basic block of SAR ADC includes sample-and-hold circuit (S/H), DAC capacitor array, comparator circuit and successive approximation controller. Generally, the SAR ADC used a binary-weighted method with sampling mode and compared mode to implement the circuit [10]. According to the comparison result of switching capacitor array, it could obtain the digital output signal as Logical High ("1") or Logical Low ("0"). In the block diagram of Fig. 1, it should be noticed that Bit n (n=1~12) will be extracted from the process of the voltage comparator and capacitor switch. Finally, the operation will repeat until the least significant bit (LSB) that is decided.

B. Processing Flow of the proposed calibration algorithm

Figure 2 shows the processing flow of the self-calibration method. According to the block diagram, it starts from a sine wave generator with frequency condition setting and then 14-bit DAC output signal is fed into the target SAR ADC. After using the calibration formula, the various analytic results with differently desired frequencies can be employed to obtain the optimized calibration result. Therefore, the behaviour of new digital calibration code is generated and the proposed algorithm can be easily implemented according to Verilog code.

C. Matlab Model Design of Recursive DFT Computation

According to Lai *et al.*'s [11], we know the z-transform formula of *N*-point recursive DFT computation can be defined as follow:

$$H(z) = \frac{W_N^k - z^{-1}}{1 - 2\cos\left(2\pi k/N\right)\times z^{-1} + z^{-2}} \quad (5)$$

$$m[n] = w_n^k \times \left(m[n-1] + x[n]\right) \quad (6)$$

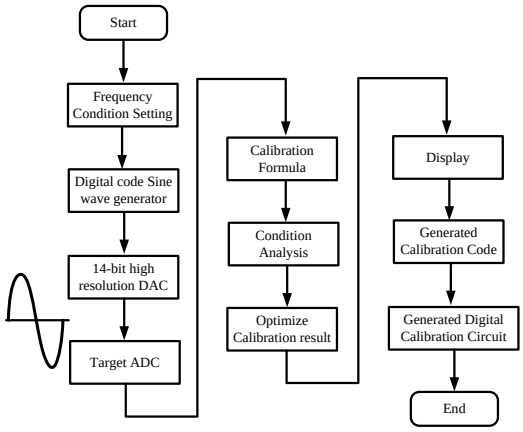


Fig. 2. The processing flow of the proposed self-calibration method.

```
Function X[k] = RDFT(x[n], TransformLength);
N = TransformLength;
DesiredFreqBin = [MainTone, 3rdTone];
for (k = 1 to length(DesiredFreqBin)){
    theta = 2*pi*DesiredFreqBin(k)/N;
    COS = cos(theta);
    SIN = sin(theta);
    a0 = 0; a1 = 0; a2 = 0; a3 = 0;
    a4 = 0; a5 = 0; a6 = 0; a7 = 0;
    for (n = 0 to N-1) {
        a0=a5+x(n);
        a1=a0*COS;
        a3=a1<<1;
        a4=a3-a2;
        if(n==N-1){
            a6=a1-a2;
            a7=a0*SIN;
            X(k)=a6+j*a7;
        }
        a5=a4;
        a2=a0;
    }
}
```

Fig. 3. The pseudo code for the function of RDFT computation.

, where x[n] is input signal and m[-1]=0. In order to reduce the multiplication of cos(θ_k), the coefficients of cos(θ_k) and 2cos(θ_k) can be shared by using the same computation, so Eq. (6) can be written as:

$$H(z)=\frac{j\sin(\theta_k)+(\cos(\theta_k)-z^{-1})}{1-z^{-1}\times(2\cos(\theta_k)-z^{-1})}. \quad (7)$$

In the targeted application, RDFT-based calibration method only needs to calculate two frequency bins, *i.e* main tone and 3rd harmonic tone as shown in Fig. 3. Therefore, the computational complexity of this RDFT algorithm totally takes (2N+2) multiplications and (4N+2) additions. In this work, RDFT design should consider the transform length and the world length of coefficient. Here, the transform length is selected to 4,096 and the word length of coefficient is set to 24 bits.

III. Simulation Result

To simulate and verify the proposed self-calibration technique, the Matlab tool is used to build the behavior model which includes the 12-bit SAR ADC, the RDFT computation, calibration formula, and generated calibration code. In addition, a 1% capacitor mismatch is adopted in the SAR ADC model to demonstrate the proposed calibration.

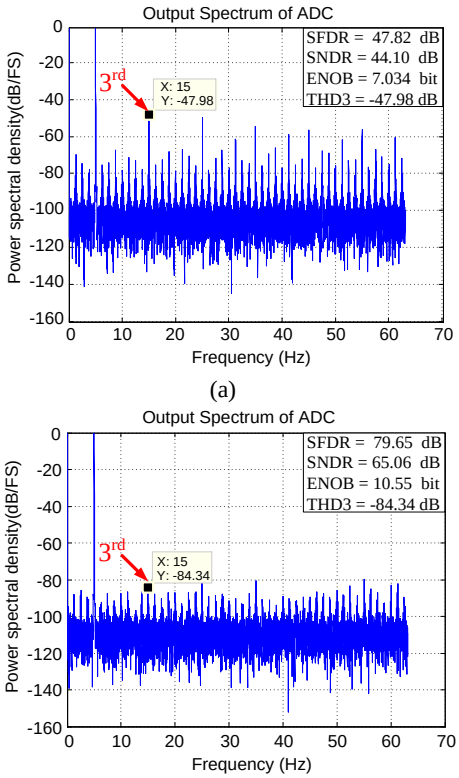
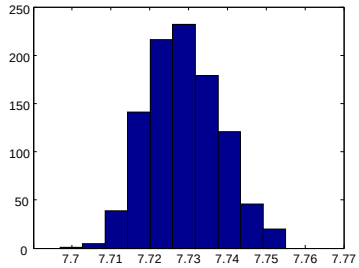


Fig. 4. Simulation result of 12-bit SAR ADC. (a) Without calibration. (b) With Calibration.

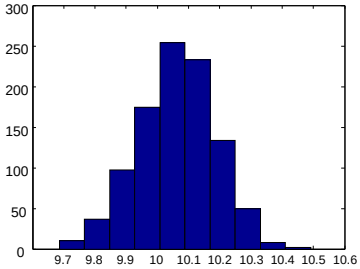
It can be easily observed that the distortion deteriorate the performance of the SAR ADC in the simulation result (Fig. 4(a)) with 5-Hz input frequency at the sampling rate of 126.26 Hz. It can be clearly found that the third harmonic tone is -47.98 dB before calibration and -84.34 dB after calibration (Fig. 4(b)). It is worth mentioning, the performance can be more effectively improved. The SNDR is enhanced from 44.10 dB to 65.06 dB, and the ENOB is improved from 7.03 bit to 10.55 bit.

Besides, we also adopt the Monte-Carlo method to analysis the performance of the SAR ADC, which includes 1% capacitor mismatch and 3σ standard deviation. We therefore combine it with the proposed model for 1000 times simulations. Fig. 5 shows the simulation results. The mean ENOB of the SAR ADC without calibration algorithm is about 7.73 bit; however, if we adopt the calibration algorithm to compensate the original data, the mean ENOB of the SAR ADC will be approximately enhanced to 10 bit. The results showed that the proposed digital calibration method can reduce the harmonic distortion and improve the performance of the ADC. Compared with other state-of-the-art technologies, the advantage of the proposed method does not require extra analog circuits and more complex algorithm such as LMS for the calibration.

Figure 6 shows the simulated ENOB with various input frequencies. According to the simulation results, the ENOB of the SAR ADC remains above 10 bit independent of different



(a)



(b)

Fig. 5. Monte-Carlo Simulation with 1% capacitor mismatch. (a) Without calibration. (b) With Calibration.

frequency ranges while the proposed calibration method is applied. Table I illustrates the comparison between the proposed method and other state-of-the-art ADCs with calibration methods. Although the performance enhancement of the proposed method is not better than that of Wang *et al.* [7], the proposed method could immediately compensate the error while the SAR ADC finished the conversion phase. On the contrary, the LMS-based algorithm [7] requires a great

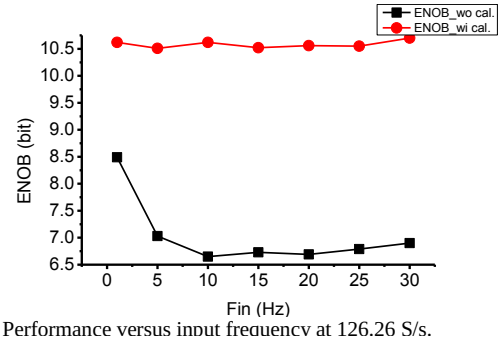


Fig. 6. Performance versus input frequency at 126.26 S/s.

number of recursive loops to make the error output become converged. This implies that it consumes more power and more calculation effort than the proposed method does.

IV. Conclusion

In this study, a digitally self-calibration method for SAR ADC is presented to compensate the error of the capacitor mismatch. The proposed method not only can help the designer to test the dynamic performance of the targeted ADC but also can compensate the ADC static error. In addition, the proposed digital calibration technique does not require any analog correction circuits and complex algorithms. According to the simulation results, the ENOB and the SFDR are, respectively, enhanced to 3.52 bit and 31.83 dB.

TABLE I
COMPARISON OF ADCS WITH DIFFERENT CALIBRATION METHODS.

Method	[5]	[7]+	[9]*	This work+
Technology	0.18 um	NA	0.18 um	NA
Method	Dither	LMS	RDFT	RDFT
Supply voltage	3.3/1.8 V (digital/analog)	NA	1.8 V	NA
Resolution	10 bit	16	12	12 bit
Sampling rate	768 kS/s	NA	200 kS/s	126.26 S/s
SNDR (dB) (Wo/Wi)	49.7 / 60.9	55.9 / 89.1	61.8 / 69.6	44.1 / 65.0
ENOB (bit) (Wo/Wi)	7.96 / 9.83	8.99 / 14.5	9.98 / 11.2	7.03 / 10.55

*Post-layout simulation result. +Behavioural result.

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